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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/676,310
Filing Date: September 30, 2003
Appellant(s): JOURDAN ET AL.

Angelo J. Gaz
Registration No. 45,907
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9 November 2006 appealing from the Office action mailed 31 May 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claim Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Sharangpani (U.S. Patent No. 6,065,115)

Rodgers (U.S. Publication No. 2003/0061258)

(9) Grounds of Rejection

Maintained Rejections

Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 6-13 and 17-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sharangpani et al. (U.S. Patent No. 6,065,115) hereinafter referred to as Sharangpani.

As per claim 1, Sharangpani discloses a method comprising: assigning an identification number (ID) (Fig. 5 tag 504) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs; determining whether one or more branches are predicted correctly; determining which of the one or more branch paths are dependent on a mispredicted branch; and determining whether one or more of the plurality of uops belong to a branch path that is dependent on the mispredicted branch based on their assigned IDs. (Col. 10 lines 6-20)

As per claim 2, Sharangpani discloses the method of claim 1, further comprising retiring a uop that belongs to the branch path dependent on the mispredicted branch. (Col. 10 line 18-20)

As per claim 6, Sharangpani discloses the method of claim 1, further comprising maintaining a list of available IDs. (Col. 10 lines 32-39)

As per claim 7, Sharangpani discloses the method of claim 6, wherein assigning an ID to each of a plurality of uops to identify a branch path to which the uop belongs comprises assigning by an allocator (Fig. 3 stream management logic 109) an ID for each of the plurality of uops from the list of available IDs. (Col. 10 lines 6-20)

As per claim 8, Sharangpani discloses the method of claim 7, further comprising stalling the allocator if there is no available ID to be assigned. (Col 10 line 61-Col. 11 line 6) *The examiner asserts that if insufficient resources are available, the processor holds an instruction stream until they become available.*

As per claim 9, Sharangpani discloses the method of claim 7, further comprising placing an ID on the list of available IDs when all uops that have been assigned that ID have been retired. (Col. 11 lines 53-61)

As per claim 10, Sharangpani discloses an apparatus comprising: an allocator (Fig. 3 stream management logic 109) to assign a plurality of micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs; (Col. 10 lines 6-20) a jump unit (Fig. 3 branch processing and prediction logic 316) coupled to the allocator to determine whether branches are predicted correctly (Col. 6 lines 53-62); and an execution unit (Fig. 3 execution logic 320) coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs. (Col. 11 lines 48-53)

As per claim 11, Sharangpani discloses the apparatus of claim 10, further comprising a retire unit (Fig. 3 retirement and write back logic 326) coupled to the jump unit to retire uops that are related to the mispredicted branch. (Col. 11 lines 48-53)

As per claim 12, Sharangpani discloses the apparatus of claim 11, wherein the allocator further maintains a list of available IDs and assigns an ID for each branch from the list of available IDs. (Col. 10 lines 32-39)

As per claim 13, Sharangpani discloses the apparatus of claim 12, wherein the retire unit is to further place an ID on the list of available IDs when all uops that have been assigned that ID have been retired. (Col. 11 lines 53-61)

As per claim 17, Sharangpani discloses the apparatus of claim 10, further comprising an instruction fetch unit (Fig. 3 fetch unit 304) coupled to the allocator to fetch a next instruction based on a next instruction pointer. (Col. 5 lines 45-50)

As per claim 18, Sharangpani discloses the apparatus of claim 17, further comprising an instruction decode unit (Fig. 3 decode unit 306) coupled to the instruction fetch unit to decode the fetched instructions. (Col. 5 lines 58-61)

As per claim 19, Sharangpani discloses a system comprising:

an input/output (I/O) controller; *The examiner asserts that Sharangpani's invention takes in input and produces output, all of which must inherently be controlled. Without an I/O controller, the device would be unable to read input or produce output, rendering the system useless.*

and a processor (Fig.1 processor 101) coupled to the I/O controller, the processor including:

an allocator (Fig. 3 stream management logic 109) to assign micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs; (Col. 10 lines 6-20)

a jump unit (Fig. 3 branch processing and prediction logic 316) coupled to the allocator to determine whether branches are predicted correctly; (Col. 6 lines 53-62)

and an execution unit (Fig. 3 execution logic 320) coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs. (Col. 11 lines 48-53)

As per claim 20, Sharangpani discloses the system of claim 19, wherein the processor further comprises a retire unit (Fig. 3 retirement and write back logic 326) coupled to the jump unit to retire uops that are related to a mispredicted branch. (Col. 11 lines 48-53)

As per claim 21, Sharangpani discloses the system of claim 19, wherein the processor further comprises an instruction fetch unit (Fig. 3 fetch unit 304) coupled to the allocator to fetch a next instruction based on a next instruction pointer. (Col. 5 lines 45-50)

As per claim 22, Sharangpani discloses the system of claim 21, wherein the processor further comprises an instruction decode unit (Fig. 3 decode unit 306) coupled to the instruction fetch unit to decode the fetched instructions. (Col. 5 lines 58-61)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-5 and 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani in view of Rodgers et al. (U.S. Patent Application Publication No. 2003/0061258) hereinafter referred to as Rodgers.

As per claims 3 and 14, Sharangpani discloses the method of claim 1 and apparatus of claim 10, but fails to disclose the processor further comprising assigning each of the plurality of uops a sequence number.

Rodgers discloses assigning each of a plurality of uops a sequence number. (Paragraph 80 lines 20-28)

Rodgers discloses that multithreaded processing "provides the potential for more effective utilization of various processor resources." Since Sharangpani's invention also executes instructions out-of-order (Sharangpani col. 6 lines 10-14), it would be desirable to have a system to ensure that all instructions are retired in a correct order to ensure proper processor functionality.

It would have been obvious to one of ordinary skill in the art at the time of invention to have included Rodgers' issue/retire scheme of assigning and using sequence numbers in Sharangpani's processor for the benefit of ensuring proper operation.

As per claims 4 and 15, Sharangpani and Rodgers disclose the method of claim 3 and apparatus of claim 14, further comprising storing the sequence number of an

oldest valid uop (Rodgers retirement pointer 180) in each branch path. (Rodgers paragraph 79 and paragraph 80 lines 20-28) *The examiner asserts that all valid uop sequence numbers are stored in the table 180, including the oldest.*

As per claims 5 and 16, Sharangpani and Rodgers disclose the method of claim 4 and apparatus of claim 15, further comprising comparing the sequence number of a uop to the sequence number of the oldest valid uop in a same branch path. *The examiner asserts that before an instruction is retired, the retirement pointer must be compared to the pending instruction.*

(10) Response to Argument

Appellant states:

"Sharangpani discloses storing a tag that associates an instruction stream with a particular instruction pointer instead of 'identifying a branch path to which the uop belongs.' This difference is best demonstrated by carefully considering how efficiently an instruction can be associated with a branch path. According to the cited language of claim 1, the branch path of a particular instruction can be found by simply looking at the tag for the instruction. However, in Sharangpani additional steps are required to find out which branch path is associated with an instruction. First, the instruction is associated with a particular stream. Second, the stream associated with an instruction pointer. Third, the instruction pointer is associated with a target instruction stream (See Sharangpani, col. 10, ll. 6-20). Therefore, in Sharangpani, at least the extra steps of determining which instruction stream is associated with the instruction pointer and associating the instruction pointer with the target instruction are necessary to associate the individual instructions of the stream with their respective branch path. The extra steps necessary to identify the branch path associated with the instruction highlights the differences between the tag in Sharangpani and the ID in the claim."

Examiner finds this argument unpersuasive for two main reasons.

First. The claim requires "assigning an identification number (ID) to each of a pulraity of micro-operations (uops) to identify a branch path to which the uop belongs."

In the citation above, Appellant admits that Sharangpani discloses this limitation within the citation above (although, appears to deny it later—see the bottom of page 6 of the Appeal Brief). Appellant goes further to say that Sharangpani requires additional steps to complete this identification and, therefore, there are differences between the current application and Sharangpani. This argument does not appear to have merit; it does not relate to the claims. Nowhere in claim 1 is there a requirement that this identification be completed in a certain amount of steps or any other requirement that would distinguish this alleged difference. The rejection remains proper.

Second. Examiner reviewed Appellant's Specification in case there is a definition that should properly be read into the claims to support Appellant's argument. The identification number is first introduced on page 5. The Specification states, "The allocator 102 determines which branch path each uop belongs and assigns an identification number (ID) to the uop based on the branch path to which the uop belongs." This is not a definition, but a feature; therefore, it is improper to read this limitation into the claimed invention. However, even if this limitation were read into the claims, Appellant's claims are not patentable over Sharangpani for two reasons: a) the feature within the claims is not consistent with the reasoning that is argued above and b) this feature is also found in Sharangpani (col 10 lines 6-21).

The arguments with respect to Claims 10-13, 17-18 and 19-22 Applicant states that these arguments are "analogous to the one...for claim 1"

Applicant states:

"[Regarding claims 3-5, the motivation is not proper] because it incorrectly assumes improper operation necessitating the incorporation of Rodger's issue/retirement scheme. However, Sharangpani discloses a way to 'ensure that all instructions are retired in a correct order to ensure proper processor functionality' without being combined with Rodgers....Hence, the Patent Office's attempt to 'combine' references is not a combination of teachings but instead a substitution of one way of doing things with another, since both teachings are superfluous."

Examiner agrees that the combination is, in some ways, a substitution; however, this does not make the obvious rejection inappropriate. Replacing one technique used completing an action with another that completes a similar action is not improper.

Regarding the motivation, Sharangpani does retire the instructions in the proper order, but gives little information regarding the technique of doing so. This makes it impossible to differentiate the nuances of each retiring technique. Still, the motivation exists for Sharangpani to utilize the teachings of Rodgers to ensure proper execution of each instruction. Additionally, the technique of Rodgers saves all required information with the instruction, making retirement analysis and debugging strategies very simple. Likely, the retirement scheme of Sharangpani was intended to be quite similar to that of Rodgers. Col 11 line 67 to col 12 line 3 of Sharangpani states, "Results produced by speculatively executed instructions from a code section identified as being an 'incorrect' code section, and thus, invalid, are not committed to the processor state." So, the instructions are marked invalid, as disclosed in Rodger (paragraph 80). In the opinion of the Examiner, however, the disclosure of Sharangpani does not give quite enough information for an anticipatory rejection of all the limitations disclosed in Applicant's claims 3-5. So, the obvious rejection in view of Rodgers appeared more appropriate.

The argument suggesting that Sharangpani did not have proper motivation to utilize the technique of Rodgers is unpersuasive.

Appellant then makes the same argument that is addressed with regard to claim 1 as a further reason that the obvious rejection for claims 3-5 is improper. The same argument is made regarding claimd 14-16.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

Brian P. Johnson

07 December 2006

Conferences:

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